[0017] Claims

1. A method of fabricating an integrated silicon-germanium heterobipolar transistor wherein between a silicon-germanium base layer and a silicon emitter layer a silicon dioxide layer is formed, characterized in that said silicon dioxide layer is formed by means of Rapid Thermal Processing (RTP).

2. The method as set forth in claim 1 wherein said silicon dioxide layer and said emitter layer are formed by means of a single continual process.

3. The method as set forth in claim 1 wherein said base layer is heated in a sequence of temperature steps to a process temperature at which said silicon dioxide layer is subsequently formed.

4. The method as set forth in claim 3 wherein in a first temperature step said base layer is heated to a temperature between 350°C and 500°C.

5. The method as set forth in claim 4 wherein said base layer is heated in a second temperature step to approximately 640°C.

6. The method as set forth in any of the claims 5 wherein said base layer 15 is heated in a third temperature step to approximately 705°C.

7. The method as set forth in claim 3 wherein said base layer is heated in a nitrogen atmosphere.

8. The method as set forth in claim 7 wherein high-purity nitrogen is used.

9. The method as set forth in claim 1 wherein said base layer 20 is exposed to an oxygen-nitrogen atmosphere for approximately 10 seconds.

10. The method as set forth in claim 1 wherein said silicon dioxide layer has a thickness between 0.3 nm and 0.4 nm, preferably approximately 0.35 nm.

11. The method as set forth in claim 1 wherein said silicon-germanium heterobipolar transistor is a pnp-bipolar transistor.

12. The method as set forth in claim 1 wherein an emitter layer is formed of polysilicon.

13. The method as set forth in claim 1 wherein the properties of said silicon dioxide layer are monitored during said RTP.

14. The method as set forth in claim 1 wherein the surface of said silicon-germanium base layer is pre-cleaned and said silicon dioxide layer is subsequently formed in a single continual process.

15. An integrated silicon-germanium heterobipolar transistor comprising a silicon-germanium base layer, a silicon emitter layer and a silicon dioxide layer arranged between said base layer and said emitter layer wherein said silicon dioxide layer is obtainable by means of Rapid Thermal Processing (RTP).

16. The integrated silicon-germanium heterobipolar transistor as set forth in claim 15 wherein said transistor is a pnp-silicon-germanium heterobipolar transistor.